IN THE CLAIMS:

1. (currently amended) A method of forming a layer of interconnect in an integrated circuit comprising the steps of:

depositing a first layer of interlayer dielectric (ILD) on a lower layer of said integrated circuit above a set of lower alignment marks;

depositing a first hardmask layer of TaN on said first layer of ILD, said first layer being substantially transparent in a relevant wavelength range in which said hardmask layer has a resistivity greater than about 400 micro Ohm-cm;

forming an upper set of alignment marks;

patterning said ILD through said hardmask layer to form a set of apertures in said ILD; and

forming a conductive interconnect in said set of apertures.

2. (currently amended) A method of forming a layer of interconnect in an integrated circuit comprising the steps of:

depositing a first layer of interlayer dielectric (ILD) on a lower layer of said integrated circuit above a set of lower alignment marks;

depositing a first hardmask layer of TaN on said first layer of ILD, said first layer being substantially transparent in a relevant wavelength range;

forming an upper set of alignment marks;

patterning said ILD through said hardmask layer to form a set of apertures in said ILD; and

forming a conductive interconnect in said set of apertures;

in which said hardmask layer is deposited by sputter deposition of Ta in an ambient containing N_2 and a carrier gas such that (N_2flow)/(N_2 + carrier flow) > 0.5.

3. (original) A method according to claim 1, in which said hardmask layer is deposited by chemical vapor deposition by reacting a precursor gas containing Ta in an ambient containing N_2.

4. (original) A method according to claim 2, in which said hardmask layer is substantially transparent in said relevant wavelength range.

5. (original) A method according to claim 3, in which said hardmask layer is substantially transparent in said relevant wavelength range.

6. (original) A method according to claim 2, in which said hardmask layer has a resistivity greater than about 400 micro Ohm-cm.

7. (Canceled)

8. (original) A method according to claim 2, in which said hardmask layer has a thickness ranging from 5nm to 100nm.

9. (original) A method according to claim 3, in which said hardmask layer has a thickness ranging from 5nm to 100nm.

10. (original) A method according to claim 2, in which said hardmask layer has a composition of less than 50% Ta.

11. (original) A method according to claim 3, in which said hardmask layer has a composition of less than 50% Ta.

12. - 22 (canceled)